REMARKS

By this amendment, claim 1, 2 and 12 have been amended and claims 1-14 are active. This amendment is filed in reply to the outstanding Final Office Action of January 27, 2005, no new matter has been added and is believed to be fully responsive thereto and reconsideration is respectfully requested.

Specification and Drawing Objections

The Examiner objected to the drawings under 37 CFR 1.83(a) and the specification under 37 CFR 1.91 because the drawings must show every feature of the invention claimed and the specification lacked an enabling description for "isolation elements". Therefore, the "isolation elements" must be shown. By this amendment Figures 1 and 2 have been changed to show the isolation elements. Additional descriptions have been added to paragraphs 19, 26 and 29 to provide the enablement of the "isolation elements". No new matter has been added since these details were added to better explain the invention as originally claimed.

Claim Objections

The Examiner objected to claims 1-11 because of certain informalities. The Examiner pointed out that the limitation in claim 1 concerning "scan chain isolation elements" and "to enable and disable BIST ..." should be combined. This amendment changes the wording of claim 1 to comply with the suggestion of the Examiner.

Rejection – 35 U.S.C. § 112

The Examiner rejected claims 1-14 under 35 U.S.C. § 112, first paragraph, as failing to comply with the enablement requirement. In particular, the Examiner pointed out that claims 1 and 12 which recited "isolation elements" were not adequately described in the specification.

The Applicants have amended the specification paragraphs 19, 26 and 29 and Figures 1 and 2 of the drawings to provide an explanation in adequate detail for the enablement of the "isolation elements".

Based on the foregoing, it is respectfully submitted that the claims are allowable under 35 U.S.C. § 112 first paragraph.

Rejection – 35 U.S.C. § 103

The Examiner rejected claims 1-14 under 35 U.S.C. § 103(a) as being unpatentable in view of Kraus et al. (US6587979). The Examiner stated that in view of the claims rejected under 35 U.S.C. § 112, first paragraph, for examination purpose, the Examiner would broadly interpret the "isolation elements" to be equivalent to a core wrapper 24 positioned near each RAM 12 for isolating logic (14,16) from the memory circuits (RAM) 12, where the wrapper includes scan chain bypass isolation elements (scan register 46) which enables and disables BIST 11, where the testing of the memory macro circuits (RAM) 12 is performed while the logic scan chain results are read out via a SCANOUT bus 23 to tester 21 by serially shifting the data outward from the logic circuits (14, 16). The Examiner also indicated that Kraus, et al. disclose scan register

(46) within each core wrapper 24 connected to lines of RAM bus 32 that convey data output of RAM12 to logic circuits (14,16).

The Applicants respectfully submit that Kraus et al. disclose nothing about simultaneous test of logic and memory. Core wrapper 24 is described in detail in Figure 5 (see Kraus Col 11 line 36). In Figure 6 we see how a pattern generator is muxed into the data and address paths of the RAM – however we do not see any isolation of the voltages of the RAM nor do we see isolation of the clocks to the RAM. The circuits shown in Figure 6 of Kraus cannot address the issues of different operating voltages and different clock frequencies between the RAM and the logic on the chip. Kraus does not verify scan chain operation by loading patterns into RAM (12) from Pattern Generator (50). Doing this operation only verifies the BIST and the RAM and only if both are functional.

Kraus, et al. teach in Col 12 lines 2-10 that asserting the FORCE signal forces data from the Scan Register (46) on the bus such that logic circuits 14, 16 see that data rather than the data from the RAM. This is bypassing the RAM itself not bypassing the latches which constitute the BIST engine as we show in our Figure 2. The bypass in our Figure 2 is for the purposes of allowing the scan chain to function while separately and simultaneously allowing the BIST latches to function in the non-scan BIST pattern generation mode. This is not what Kraus, et al. teach by their Scan Force Mode and Scan Capture Mode which are to test that the BIST Logic works correctly.

Kraus, et al. may teach that both logic and memory can be tested. However, Kraus, et al. do not teach that both logic and memory can be tested simultaneously; the memory being tested by the BIST engine having had the BIST engines clock and scan latches isolated from the logic as well as the memory's voltage having been isolated from

the logic to allow it to be tested at independent conditions; the logic being tested by scan methods using its isolated clock scan chains and voltages.

In fact, Kraus, et al. cannot test both logic and memory at independent conditions because the voltages for memory and logic are tied together as well as the clocks for both memory and logic are tied together. Kraus, et al. do not even show the clocking for the latches that comprise either BIST engine or the logic.

. . . It appears that the Examiner interprets the Core Wrapper (24) as the isolation elements. However, the Core Wrapper (24) is in the wrong place. Clock isolation needs to be done within the BIST Controller as it is the BIST Controller which determines the rate at which the RAM is tested. Similarly, the scan latches within the BIST (our Figure 2 (element 44)) are what is needed to be isolated from the scan chains of the logic.

Since Kraus, et al. cannot be interpreted to show or describe or suggest the use of Voltage Isolation for simultaneous testing of memory and logic, it is therefore clear to make the claims 1-14 not obvious using Kraus, et al.

Accordingly, it is respectfully submitted that claims 1-14 should be allowable under 35 U.S.C. § 103.

Conclusion

Based on the foregoing, it is respectfully submitted that all the claims active in the subject patent application are in condition for allowance and that the application may be passed to issuance.

The Examiner is urged to call the undersigned at the number listed below if, in the Examiner's opinion, such a phone conference would aid in furthering the prosecution of this application.

Respectfully submitted,

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